PATENT ABSTRACTS OF JAPAN

(11)Publication number : 2003-101080
(43)Date of publication of application : 04.04.2003

(51)Int.Cl. H01L 33/00
H01L 23/12
H01L 31/02
H01S 5/022
H05K 1/02
H05K 1/18
H05K 3/46
// H05K 1/14

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(21)Application number : 2001-293858
(22)Date of filing : 26.09.2001

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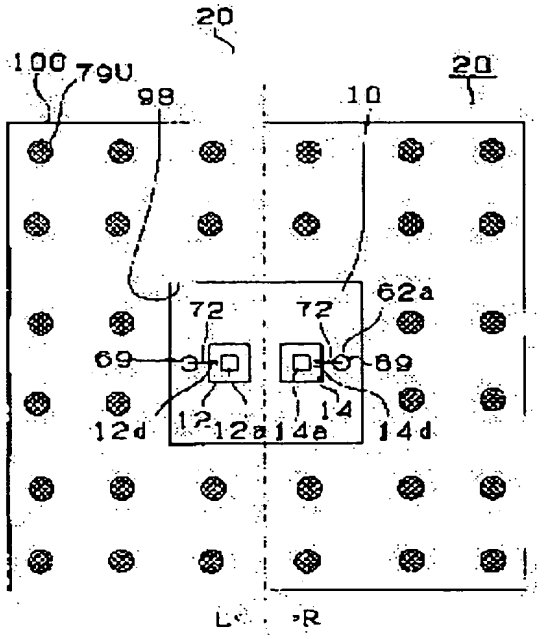
(54) BOARD FOR IC CHIP MOUNTING

(57)Abstract:
PROBLEM TO BE SOLVED: To provide a board for IC chip mounting, on which a light-receiving element, a light-emitting element, and an IC chip can be connected rationally.
SOLUTION: On a side L of the board 20 for IC chip mounting where the light-emitting element 12 is mounted, a conductor circuit is arranged which mainly connects the light-emitting element 12 and IC chip and on the side R, where the light receiving element 14 is mounted, a conductor circuit is arranged which mainly connects the light-receiving element 14 and IC chip. The conductor circuit, which connects the light-receiving element 13 and IC chip and the conductor circuit which connects the light-emitting element 12 and IC chip become short in length and the light-receiving element, light-emitting element, and IC chip can be connected rationally.



LEGAL STATUS

[Date of request for examination]

[Date of sending the examiner's decision of rejection]

[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]

[Date of final disposal for application]

[Patent number]

[Date of registration]

[Number of appeal against examiner's decision of rejection]

[Date of requesting appeal against examiner's decision

of rejection]
[Date of extinction of right]

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CLAIMS

[Claim(s)]
[Claim 1] a core substrate — the resin insulating layer between layers, and a conductor — to the multilayer printed wiring board with which the laminating of the conductor layer which consists of a circuit is carried out by turns, and it changes It is the substrate for IC chip mounting which mounts IC chip while carrying the 1st component and 2nd component. A circuit is arranged. the conductor which mainly connects the 1st component and IC chip to said 1st said multilayer printed wiring board component loading-side — the conductor which mainly connects the 2nd component and IC chip to said 2nd said multilayer printed wiring board component loading-side — the substrate for IC chip mounting characterized by having arranged the circuit.
[Claim 2] a core substrate — the resin insulating layer between layers, and a conductor — to the multilayer printed wiring board with which the laminating of the conductor layer which consists of a circuit is carried out by turns, and it changes It is the substrate for IC chip mounting which mounts IC chip while carrying a light emitting device and a photo detector. A circuit is arranged. the conductor which mainly connects a light emitting device and IC chip to said said multilayer printed wiring board light emitting device loading-side — the conductor which mainly connects a photo detector and IC chip to said said multilayer printed wiring board photo detector loading-side — the substrate for IC chip mounting characterized by having arranged the circuit.

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to a semiconductor device, and IC chip and the substrate for IC chip mounting which mounts an optical element and IC chip especially on a substrate.
[0002]
[Description of the Prior Art] In recent years, attentions have gathered for the optical fiber focusing on the communication link field. In especially IT (information technology) field, the communication technology which used the optical fiber for maintenance of the high-speed Internet network is needed. In the communication system using the optical fiber which has the descriptions, such as ** low loss, ** high bandwidth, ** narrow diameter and a light weight, no ** guiding, and ** saving resources, and has this description, compared with the communication system using the conventional metallic cable, the number of repeaters can be reduced sharply, construction and maintenance become easy, and an optical fiber can attain economization of communication system, and high-reliability-ization.
[0003] Moreover, since an optical fiber can multiplex the light of the wavelength from which not only the light of one wavelength but many differ to coincidence with one optical fiber, it can realize the transmission line of the large capacity which can respond to a busy application, and can respond to image service etc.
[0004] Then, in network communication, such as such the Internet, using not only for the communication link of a backbone but for the communication link with a backbone and terminal equipments (a personal computer, mobile one, game, etc.) and the communication link of terminal equipments the optical communication used with the optical fiber is proposed.
[0005] Thus, when using optical communication for the communication link with a backbone and a terminal equipment etc., in order for IC which performs information (signal) processing in a terminal equipment to operate with an electrical signal, it is necessary to attach the equipment (henceforth light/electric transducer) which changes the lightwave signal and electrical signal of optical -> electric transducer, electric -> phototransducer, etc. into a terminal equipment. Mounting optics which process a lightwave signal, such as a photo detector and a light emitting device, in one substrate, connecting electric wiring and optical waveguide to these, and performing a signal transmission and signal processing with IC chip, with this terminal equipment, is examined.
[0006]
[Problem(s) to be Solved by the Invention] the case where a photo detector and a light emitting device are mounted in the substrate of 1 which constitutes light/electric transducer with IC chip here — one side — IC chip — mounting — on the other hand — alike — a photo detector and a light emitting device — mounting — the conductor in a substrate — IC chip, a photo detector, and a light emitting device will be connected through a circuit (wiring). however — how — a conductor — if a circuit is arranged, whether IC chip, a photo detector, and a light emitting device can be connected rationally will pose a problem.
[0007] The place which it is made in order that this invention may solve the technical problem mentioned above, and is made into the purpose is to offer the substrate for IC chip mounting which can connect rationally a photo detector, a light emitting device, and IC chip.
[0008]
[Means for Solving the Problem] in order to solve the above-mentioned technical problem — claim 1 — a core substrate — the resin insulating layer between layers, and a conductor — to the multilayer printed wiring board with which the laminating of the conductor layer which consists of a circuit is carried out by turns, and it changes It is the substrate for IC chip mounting which mounts IC chip while carrying the 1st component and 2nd component. the conductor which mainly connects the 1st component and IC chip to said 1st said multilayer printed wiring board component loading-side — the conductor which arranges a circuit and mainly connects the 2nd component and IC chip to said 2nd said multilayer printed wiring board component loading-side — it makes

to have arranged the circuit into a technical feature.
[0009] the conductor which mainly connects the 1st component and IC chip to a 1st multilayer printed wiring board component loading-side in claim 1 — the conductor which arranges a circuit and mainly connects the 2nd component and IC chip to a 2nd multilayer printed wiring board component loading-side — a circuit is arranged. for this reason, the conductor which connects the 1st component and IC chip — the conductor which connects the die length, and the 2nd component and IC chip of a circuit — the die length of a circuit becomes short and the 1st component, 2nd component, and IC chip can be connected rationally.
[0010] moreover, claim 2 — a core substrate — the resin insulating layer between layers, and a conductor — to the multilayer printed wiring board with which the laminating of the conductor layer which consists of a circuit is carried out by turns, and it changes It is the substrate for IC chip mounting which mounts IC chip while carrying a light emitting device and a photo detector. the conductor which mainly connects a light emitting device and IC chip to said said multilayer printed wiring board light emitting device loading-side — the conductor which arranges a circuit and mainly connects a photo detector and IC chip to said said multilayer printed wiring board photo detector loading-side — it makes to have arranged the circuit into a technical feature.
[0011] the conductor which mainly connects a light emitting device and IC chip to a multilayer printed wiring board light emitting device loading-side in claim 2 — the conductor which arranges a circuit and mainly connects a photo detector and IC chip to a multilayer printed wiring board photo detector loading-side — a circuit is arranged. for this reason, the conductor which connects a photo detector and IC chip — the conductor which connects the die length, and a light emitting device and IC chip of a circuit — the die length of a circuit becomes short and a photo detector, a light emitting device, and IC chip can be connected rationally. moreover, the conductor which transmits the input from a photo detector — the conductor which delivers the output to a light emitting device a circuit — effect of a noise etc. can be made hard to separate I/O and to affect it, in order to divide and arrange a circuit within a multilayer printed wiring board. It is especially useful at the time of a package substrate and **.
[0012]
[Embodiment of the Invention] The manufacture approach of the substrate for IC chip mounting which constitutes the substrate for optical element mounting of this invention passes both through lamination and a further predetermined process, after producing separately the substrate for optical element insertion, and a package substrate. Then, in this specification, how to produce the substrate for optical element insertion and the approach of producing a package substrate are first explained separately in order of a process, respectively, and the process which sticks both and is used as the substrate for IC chip mounting is explained after that.
[0013] (a) production of the substrate for optical element insertion — both sides Of Substrate a — a conductor — the conductor whose above-mentioned substrate a was pinched while forming the circuit — the conductor which forms the through hole which connects between circuits — perform a circuit formation process (a). forming a solid conductor layer and specifically performing etching processing to a conductor layer in the shape of a pattern subsequently to by performing nonelectrolytic plating processing etc. to the whole front face of the substrate a containing the wall surface of this through tube, after forming a through tube in Substrate a by drilling, the lasing, etc. — a conductor — the conductor the circuit and whose substrate a were pinched — the through hole which connects between circuits can be formed. moreover, the thing for which nonelectrolytic plating processing etc. is performed to the wall surface of this through tube, and etching processing is further performed to a conductor layer after forming a through tube in the substrate with which the solid conductor layer was formed beforehand — a conductor — a circuit and a through hole may be formed.
[0014] moreover, the thing which plating resist is formed in a part of front face of Substrate a, and a conductor layer is formed by performing nonelectrolytic plating processing, nonelectrolytic plating processing, electrolysis plating processing, etc. subsequently to the wall surface and the plating-resist agenesis section of a through tube, and is further exfoliated in plating resist after forming a through tube in Substrate a — a conductor — a circuit and a through hole may be formed. Moreover, in this process, after forming a through tube in Substrate a, it is desirable to perform DESUMIA processing to this through tube. For example, drug solution processing, dry processing using the plasma, etc. are mentioned, using oxidizers, such as permanganic acid and a chromic acid, as the above-mentioned DESUMIA processing.
[0015] As the above-mentioned substrate a, the substrate with which reinforcing materials, such as a glass fiber, consist of resin (for example, glass epoxy resin) with which it sank in, FR-4 substrate, FR-5 substrate, etc. are mentioned to an epoxy resin, polyester resin, polyimide resin, bismaleimide-triazine resin (BT resin), phenol resin, and these resin, for example. Moreover, a double-sided copper-clad laminated circuit board, an one side copper-clad laminated circuit board, a RCC substrate, etc. may be used as a substrate with which the solid conductor layer was formed. in addition, a conformal substrate and the substrate formed with the additive process — a conductor — the processing which uses as a substrate with which the circuit was formed and a through tube

forms in this substrate, and the processing which forms the conductor layer of that wall surface — giving — a conductor — a circuit and a through hole may be formed.

[0016] After forming the above-mentioned through hole, it is desirable for it to be filled up with a resin filler and to form a resin filler layer in this through hole. In addition, restoration of a resin filler can lay on a substrate the mask with which opening was formed in the part equivalent to a through hole, and can be performed using a squeegee. Moreover, when filled up with a resin filler in a through hole, it is desirable to form a roughening side in the wall surface of a through hole before restoration. Thereby, it is because the adhesion of a through hole and a resin filler layer improves more.

[0017] As the above-mentioned resin filler, the resin constituent containing an epoxy resin, a curing agent, and an inorganic particle etc. is **********, for example. Although not limited especially as the above-mentioned epoxy resin, a kind is [choose / from the group which consists of a bisphenol mold epoxy resin and a novolak mold epoxy resin] desirable in it being few. It is because a novolak mold epoxy resin is excellent in thermal resistance or chemical resistance with high intensity, the viscosity can be prepared even if a diluent solvent is not used for a bisphenol mold epoxy resin by choosing the resin of A mold or a female mold, it is not disassembled even if it is among strong base nature solutions, such as nonelectrolytic plating liquid, and it is hard to carry out a pyrolysis.

[0018] As the above-mentioned bisphenol mold epoxy resin, the bisphenol A mold epoxy resin and a bisphenol female mold epoxy resin are desirable, and the point which is hypoviscosity and can be used with a non-solvent to a bisphenol female mold epoxy resin is more desirable. Moreover, as the above-mentioned novolak mold epoxy resin, a kind is [choose / from a phenol novolak mold epoxy resin and a cresol novolak mold epoxy resin] desirable in it being few.

[0019] Moreover, a bisphenol mold epoxy resin and a cresol novolak mold epoxy resin may be mixed and used. In this case, as for the mixed ratio of a bisphenol mold epoxy resin and a cresol novolak mold epoxy resin, it is desirable that it is 1 / 1 - 1/100 in a weight ratio.

[0020] It is not limited especially as a curing agent contained in the above-mentioned resin filler, a well-known curing agent can be used conventionally, for example, an imidazole system curing agent, an acid-anhydride curing agent, an amine system curing agent, etc. are mentioned. In these, an imidazole system curing agent is desirable and liquefied 1-benzyl-2-methylimidazole, and 1-cyanoethyl-2-ethyl-4-methylimidazole and a 4-methyl-2-ethyl imidazole are desirable in 25 degrees C especially.

[0021] Moreover, as an inorganic particle contained in the above-mentioned resin filler, what consists of silicon compounds, such as magnesium compounds, such as potassium compounds, such as lime compounds, such as aluminium compounds, such as an alumina and an aluminum hydroxide, a calcium carbonate, and a calcium hydroxide, and potassium carbonate, a magnesia, a dolomite, basic magnesium carbonate, and talc, a silica, and a zeolite, etc. is mentioned, for example. These may be used independently and may be used together two or more sorts. Moreover, coating of the above-mentioned inorganic particle may be carried out by the silane coupling agent etc. It is because the adhesion of an inorganic particle and an epoxy resin improves.

[0022] Moreover, the content ratio in the resin constituent of the above-mentioned inorganic particle has 10 - 80 desirable % of the weight, and its 20 - 70 % of the weight is more desirable. It is because adjustment of a coefficient of thermal expansion can be aimed at between substrates etc. if it is this range.

[0023] Moreover, especially the configuration of the above-mentioned inorganic particle is not limited, but the shape of a globular shape, an ellipse globular shape, the letter of crushing, and a polyhedron etc. is mentioned. In these, the shape of the shape of a ball or an ellipse ball is desirable. It is because generating of the crack resulting from the configuration of a particle etc. can be controlled. The mean particle diameter of the above-mentioned inorganic particle has desirable 0.1-5.0 micrometers.

[0024] Moreover, in the above-mentioned resin constituent, other thermosetting resin, thermoplastics, etc. may be contained in addition to the above-mentioned epoxy resin etc. As the above-mentioned thermosetting resin, polyimide resin, phenol resin, etc. are mentioned, for example. As the above-mentioned thermoplastics For example, a polytetrafluoroethylene (PTFE) and ethylene tetrafluoride 6 fluoride propylene copolymer (FEP), Fluororesins, such as an ethylene tetrafluoride perphloro alkoxy copolymer (PFA), Polyethylene terephthalate (PET), polysulfone (PSF), A polyphenylene sulfide (PPS), thermoplastic mold polyphenylene ether (PPE), Polyether sulfone (PES), polyether imide (PEI), polyphenylene sulfone (PPES), polyethylenenaphthalate (PEN), a polyether ether ketone (PEEK), polyolefine system resin, etc. are mentioned. These may be used independently and may use two or more sorts together. In addition, it may replace with the above-mentioned epoxy resin, and these resin may be used.

[0025] moreover, this conductor — in a circuit formation process, after forming a resin filler layer in a through hole, it is desirable to form a wrap lid plating layer for the exposure from the through hole of this resin filler layer. It is because it becomes possible to form a solder pad by forming a lid plating layer not only the land top of a

through hole but on a lid plating layer, so the degree of freedom of a design improves more.
[0026] After the above-mentioned lid plating layer forms a conductor layer in the front face of the substrate containing the exposure of for example, a resin filler layer and forms etching resist in a lid plating stratification part, it performs etching processing, or forms plating resist in the lid plating layer agenesis part beforehand, and can form it by performing plating processing and removal of plating resist.
[0027] therefore, this conductor — processing in the following procedure in a circuit formation process, in forming a lid plating layer on a through hole — a conductor — formation of a circuit and a through hole and formation of a lid plating layer can be performed to coincidence. That is, first, after forming a through tube in a substrate, a conductor layer is formed in the front face of the substrate containing the wall surface of this through tube, and, subsequently to the wall surface, it is filled up with a resin filler in the through tube in which the conductor layer was formed. furthermore, the conductor after carrying out laminating formation of the conductor layer by plating processing etc. on the conductor layer formed in the exposure and substrate front face of a resin filler — carrying out etching removal of the conductor layer of the circuit agenesis section and the through hole agenesis section — a conductor — formation of a circuit and a through hole and formation of a lid plating layer can be performed to coincidence.
[0028] (b) next, a conductor — the conductor of one side of the substrate a in which the circuit was formed — perform the adhesives layer formation process which forms an adhesives layer in a part of circuit agenesis section [at least]. in addition, this specification — setting — the land part of a through hole — a conductor — it shall contain in a circuit therefore, the land part of a through hole — a conductor — it is not equivalent to the circuit agenesis section. the near conductor stuck with the package substrate of Substrate a at this process — an adhesives layer is formed in all or a part of circuit agenesis sections. What is necessary is just to apply the above-mentioned adhesives layer so that sufficient adhesive property with a package substrate may be acquired. Therefore, it is ** [it may form an adhesives layer in the part in which a through tube is formed at the process of (c) mentioned later].
[0029] As the above-mentioned adhesives, thermosetting resin, thermoplastics, a photopolymer, the resin with which a part of heat-curing radical was sensitization-ized, the thing which consists of these complex can be used, for example. As an example, an epoxy resin, phenol resin, polyimide resin, BT resin, etc. are mentioned, for example. Moreover, the adhesives fabricated in the shape of a sheet may be used beforehand.
[0030] (c) Next, perform the through-hole formation process which forms a through tube in some substrates a in which the adhesives layer was formed. In the through tube formed here, an optical element will be arranged in a back process. For example, router processing etc. can perform formation of the above-mentioned through tube. Moreover, although especially the formation location of the above-mentioned through tube is not limited, it is usually formed in the center of a substrate.
[0031] moreover, the above-mentioned through-hole formation process — after being and forming a through tube, in order to remove the weld flash which exists in a through tube wall surface, drug solution processing, polish processing, etc. may be performed. The above-mentioned drug solution processing can be performed using the oxidizer which consists of water solutions, such as a chromic acid and a permanganate. Such (a) The substrate for optical element insertion is producible by passing through the process of - (c).
[0032] Next, the production approach of a package substrate is explained.
(A) production of a package substrate — first — both sides Of Substrate A — a conductor — the first conductor which forms a circuit — perform a circuit formation process (A). This process can be performed by the same approach as the process of (a) of production of the substrate for optical element insertion mentioned above, for example. In addition, as a substrate A, the same thing as the substrate a mentioned above can be used, for example.
[0033] moreover, the conductor whose above-mentioned substrate A was pinched if needed — the through hole which connects between circuits may be formed. The above-mentioned through hole is formed by performing nonelectrolytic plating processing etc. to the wall surface of this through tube, after forming a through tube in the above-mentioned substrate A by drilling, the lasing, etc. Moreover, when a through hole is formed, it is desirable to be filled up with a resin filler in this through hole. In addition, restoration of a resin filler can lay on a substrate the mask with which opening was formed in the part equivalent to a through hole, and can be performed using a squeegee.
[0034] moreover, a conductor — roughening formation processing may be performed to a circuit front face (the land front face of a through hole is included). a conductor — it is because adhesion with the resin insulating layer between layers which carries out laminating formation at a back process by making a circuit front face into a roughening side can be raised. as the above-mentioned roughening formation processing — melanism (oxidization) — the etching processing using the etching reagent containing - reduction processing, the second copper complex, and an organic-acid salt etc., processing by the Cu-nickel-P needlelike alloy plating, etc. are

mentioned. In addition, before this roughening formation processing is filled up with a resin filler in a through hole, it may be performed, and it may form a roughening side also in the wall surface of a through hole. It is because the adhesion of a through hole and a resin filler improves.

[0035] The same thing as the resin filler used, for example in the process which produces the substrate for optical element insertion as a resin filler with which it is filled up in the above-mentioned through hole in case it is filled up with the inside of a through hole is mentioned.

[0036] (B) next, the above — a conductor — while forming the resin insulating layer between layers which has the Bahia hall on the substrate A in which the circuit was formed — the above-mentioned resin insulating-layer top between layers — a conductor — perform the resin insulation regular placing layer process between layers (B) which forms a circuit. Specifically, it can carry out by passing through the process of following (i) - (**). namely, (i) — first — a conductor — the resin layer which forms the non-hardened resin layer which consists of thermosetting resin or resin complex on the substrate A in which the circuit was formed, or consists of thermoplastics is formed. The resin layer which is not hardened [above-mentioned] may apply non-hardened resin by the roll coater, a curtain coating machine, etc., may fabricate it, and may carry out thermocompression bonding of the resin film non-hardened (semi-hardening), and may form it. Furthermore, the resin film with which metal layers, such as copper foil, were formed in one side of a non-hardened resin film may be stuck. Moreover, as for the resin layer which consists of thermoplastics, it is desirable to form by carrying out thermocompression bonding of the resin Plastic solid fabricated in the shape of a film.

[0037] In applying the resin which is not hardened [above-mentioned], it performs heat-treatment, after applying resin. Heat curing of the non-hardened resin can be carried out by performing the above-mentioned heat-treatment. In addition, the above-mentioned heat curing may be performed after forming opening for the Bahia halls mentioned later.

[0038] As an example of the thermosetting resin used in formation of such a resin layer, an epoxy resin, phenol resin, polyimide resin, polyester resin, a bismaleimide resin, polyolefine system resin, polyphenylene ether resin, etc. are mentioned, for example.

[0039] As the above-mentioned epoxy resin, a cresol novolak mold epoxy resin, the bisphenol A mold epoxy resin, a bisphenol female mold epoxy resin, a phenol novolak mold epoxy resin, an alkylphenol novolak mold epoxy resin, a biphenol female mold epoxy resin, a naphthalene mold epoxy resin, a dicyclopentadiene mold epoxy resin, the epoxidation object of the condensate of phenols and the aromatic aldehyde which has a phenolic hydroxyl group, triglycidyl isocyanurate, cycloaliphatic epoxy resin, etc. are mentioned, for example. These may be used independently and may be used together two or more sorts. Thereby, it excels in thermal resistance etc.

[0040] As the above-mentioned polyolefine system resin, the copolymer of polyethylene, polystyrene, polypropylene, a polyisobutylene, polybutadiene, polyisoprene, cycloolefin system resin, and these resin etc. is mentioned, for example.

[0041] Moreover, as the above-mentioned thermoplastics, phenoxy resin, polyether sulfone, polysulfone, etc. are mentioned, for example. Moreover, as complex (resin complex) of thermosetting resin and thermoplastics, especially if thermosetting resin and thermoplastics are included, it will not be limited, but as the example, the resin constituent for roughening side formation etc. is mentioned, for example.

[0042] That by which the matter of fusibility was distributed to the roughening liquid which consists of at least one sort chosen from an acid, alkali, and an oxidizer into the heat-resistant-resin matrix which is not hardened [poorly soluble] to the roughening liquid which consists of at least one sort chosen from an acid, alkali, and an oxidizer as the above-mentioned resin constituent for roughening side formation, for example is mentioned. In addition, when the same time amount immersion is carried out, the word of the above "poor solubility" and "fusibility" says relatively what has an early dissolution rate as "fusibility" to the same roughening liquid for convenience, and calls "poor solubility" relatively what has a late dissolution rate to it for convenience.

[0043] In case the above-mentioned roughening liquid is used for the resin insulating layer between layers and a roughening side is formed as the above-mentioned heat-resistant-resin matrix, what can hold the configuration of a roughening side is desirable, for example, thermosetting resin, thermoplastics, these complex, etc. are mentioned. Moreover, you may be a photopolymer. In the process which forms opening for the Bahia halls mentioned later, it is because opening can be formed by the exposure development.

[0044] As the above-mentioned thermosetting resin, an epoxy resin, phenol resin, polyimide resin, polyolefin resin, a fluororesin, etc. are mentioned, for example. Moreover, the resin which made the heat-curing radical acrylic(meta)—ization-react to these thermosetting resin using the resin which gave photosensitivity, i.e., a methacrylic acid, an acrylic acid, etc., may be used. The acrylate (meta) of an epoxy resin is desirable and, specifically, the epoxy resin which has two or more epoxy groups in 1 molecule is more more desirable still.

[0045] As the above-mentioned thermoplastics, phenoxy resin, polyether sulfone, polysulfone, polyphenylene sulfone, polyphenylene sulfide, POJIFENIRUETERU, polyether imide, etc. are mentioned, for example. These may

be used independently and may be used together two or more sorts.
[0046] As matter of the above-mentioned fusibility, an inorganic particle, a resin particle, metal particles, a rubber particle, liquid phase resin, liquid phase rubber, etc. are mentioned, for example. These may be used independently and may be used together two or more sorts.
[0047] As the above-mentioned inorganic particle, what consists of silicon compounds, such as magnesium compound; silicas, such as potassium compound; magnesias [, such as lime compound; potassium carbonate,], such as aluminium compound; calcium carbonates, such as an alumina and an aluminum hydroxide, and a calcium hydroxide, a dolomite, basic magnesium carbonate, and talc, and a zeolite, etc. is mentioned, for example. These may be used independently and may be used together two or more sorts. Dissolution removal of the above-mentioned alumina particle can be carried out by fluoric acid, and dissolution removal of the calcium carbonate can be carried out with a hydrochloric acid. Moreover, dissolution removal of a sodium content silica or the dolomite can be carried out in an alkali water solution.
[0048] As the above-mentioned resin particle, what consists of thermosetting resin, thermoplastics, etc. is mentioned, for example. When immersed in the roughening liquid which consists of at least one sort chosen from an acid, alkali, and an oxidizer It will not be limited especially if a dissolution rate is earlier than the above-mentioned heat-resistant-resin matrix. Specifically For example, what consists of amino resin (melamine resin, a urea-resin, guanamine resin, etc.), an epoxy resin, phenol resin, phenoxy resin, polyimide resin, polyphenylene resin, polyolefin resin, a fluororesin, bismaleimide-triazine resin, etc. is mentioned. These may be used independently and may be used together two or more sorts. In addition, the above-mentioned resin particle needs to carry out hardening processing beforehand. It is because the above-mentioned resin particle dissolves in the solvent in which a resin matrix is dissolved, so homogeneity will be mixed and dissolution removal only of the resin particle can be alternatively carried out neither with an acid nor an oxidizer, unless it makes it harden.
[0049] As the above-mentioned metal particles, what consists of gold, silver, copper, tin, zinc, stainless steel, aluminum, nickel, iron, lead, etc. is mentioned, for example. These may be used independently and may be used together two or more sorts. Moreover, the surface may be covered with resin etc. in order that the above-mentioned metal particles may secure insulation.
[0050] (**) Next, in forming the resin insulating layer between layers using thermosetting resin and resin complex as the ingredient, while performing hardening processing to a non-hardened resin layer, opening for the Bahia halls is formed and it considers as the resin insulating layer between layers. As for the above-mentioned opening for the Bahia halls, forming by the lasing is desirable. The above-mentioned lasing may be performed before the above-mentioned hardening processing, and may be performed after hardening processing. Moreover, when the resin insulating layer between layers which consists of a photopolymer is formed, opening for the Bahia halls may be prepared by performing exposure and a development. In addition, exposure and a development are performed before the above-mentioned hardening processing in this case.
[0051] Moreover, when forming the resin insulating layer between layers using thermoplastics as the ingredient, opening for the Bahia halls can be formed in the resin layer which consists of thermoplastics by the lasing, and it can consider as the resin insulating layer between layers.
[0052] At this time, carbon dioxide gas laser, excimer laser, UV laser, an YAG laser, etc. are mentioned as laser to be used, for example. These may be properly used in consideration of the configuration of opening for the Bahia halls to form etc.
[0053] When forming the above-mentioned opening for the Bahia halls, much openings for the Bahia halls can be formed at once by irradiating the laser beam by the excimer laser of a hologram method through a mask. Moreover, when opening for the Bahia halls is formed using the carbon dioxide gas laser of a short pulse, there is little resin remainder in opening and the damage to the resin of an opening periphery is small.
[0054] Moreover, when irradiating a laser beam through an optical-system lens and a mask, numerous openings for the Bahia halls can be formed at once. By minding an optical-system lens and a mask, it is the same reinforcement and is because whenever [illuminating-angle] can irradiate the same laser beam at coincidence at two or more parts.
[0055] (**) Next, a roughening side is formed in the front face of the resin insulating layer between layers including the wall of opening for the Bahia halls using an acid or an oxidizer if needed. In addition, this roughening side is formed in order to raise the adhesion of a glabella resin insulating layer and the thin film conductor layer formed on it, and when there is adhesion sufficient between the resin insulating layer between layers and a thin film conductor layer, it is not necessary to form it.
[0056] As the above-mentioned acid, a sulfuric acid, a nitric acid, a hydrochloric acid, a phosphoric acid, formic acid, etc. are mentioned, and permanganates, such as a chromic acid, chromate acid mixture, and sodium permanganate, etc. are mentioned as the above-mentioned oxidizer. Moreover, after forming a roughening side, it is desirable to neutralize the front face of the resin insulating layer between layers using water solutions,

neutralization liquid, etc., such as alkali. It is because it can avoid having effect of an acid or an oxidizer on degree process. Moreover, formation of the above-mentioned roughening side may be performed using plasma treatment etc.

[0057] Moreover, the maximum roughness Rmax of the above-mentioned roughening side has desirable 0.1-20 micrometers. if Rmax exceeds 20 micrometers — the roughening side itself — damage and exfoliation — winning popularity — easy — Rmax — less than 0.1 micrometers — a conductor — it is because adhesion with a circuit cannot be acquired enough. especially — a semiadditive process — a conductor — when forming a circuit, the above-mentioned maximum roughness Rmax has desirable 0.1-5 micrometers. While adhesion with a thin film conductor layer is fully securable, it is because removal of a thin film conductor layer is easy.

[0058] (**) Next, a thin film conductor layer is formed in the front face of the resin insulating layer between layers which prepared opening for the Bahia halls. The above-mentioned thin film conductor layer can be formed using approaches, such as nonelectrolytic plating, sputtering, and vacuum evaporationo. In addition, when a roughening side is not formed in the front face of the resin insulating layer between layers, as for the above-mentioned thin film conductor layer, forming by sputtering is desirable. In addition, in forming a thin film conductor layer with nonelectrolytic plating, it gives the catalyst beforehand to the galvanized front face. As the above-mentioned catalyst, a palladium chloride etc. is mentioned, for example.

[0059] Although especially the thickness of the above-mentioned thin film conductor layer is not limited, when this thin film conductor layer is formed with nonelectrolytic plating, 0.6-1.2 micrometers is desirable, and when it forms by sputtering, 0.1-1.0 micrometers is desirable. Moreover, as the quality of the material of the above-mentioned thin film conductor layer, Cu, nickel, P, Pd, Co, W, etc. are mentioned, for example. In these, Cu and nickel are desirable.

[0060] (**) Next, a dry film is used for the part on the above-mentioned thin film conductor layer, plating resist is formed, after that, electrolysis plating is performed by making the above-mentioned thin film conductor layer into a plating bar, and an electrolysis plating layer is formed in the above-mentioned plating-resist agenesis section.

[0061] Moreover, opening for the Bahia halls is filled up with this process with electrolysis plating, and it is good also considering the structure of the Bahia hall as field beer structure, and the Bahia hall which has a hollow is once formed in that top face, this hollow is filled up with a conductive paste after that, and it is good also as field beer structure. Moreover, after forming in a top face the Bahia hall which has a hollow, the hollow is filled up with a resin filler etc., a lid plating layer is further formed on it, and it is good also as a Bahia hall where a top face is flat. The Bahia hall can be formed in right above [of the Bahia hall] by making structure of the Bahia hall into field beer structure.

[0062] (**) — the conductor which exfoliated plating resist, removed further the thin film conductor layer which existed under plating resist by etching, and became independent — it considers as a circuit. As an etching reagent, persulfate water solutions, such as a sulfuric-acid-hydrogen-peroxide-solution solution and ammonium persulfate, a ferric chloride, a cupric chloride, a hydrochloric acid, etc. are mentioned, for example. Moreover, the mixed solution containing the second copper complex mentioned above as an etching reagent and an organic acid may be used.

[0063] moreover, the thing for which it replaces with the approach of performing removal with plating resist and a thin film conductor layer, and the following approaches are used after forming plating resist on the above-mentioned thin film conductor layer and forming an electrolysis plating layer in the plating-resist agenesis section — a conductor — a circuit may be formed. namely, the conductor which used the dry film for the part on this electrolysis plating layer, formed etching resist, removed an etching-resist agenesis subordinate's electrolysis plating layer and thin film conductor layer by etching after that, and became independent by exfoliating etching resist further after forming an electrolysis plating layer the whole surface on the above-mentioned thin film conductor layer — a circuit may be formed.

[0064] while forming the resin insulating layer between layers which has the Bahia hall by using such an approach — the resin insulating-layer top between layers — a conductor — the resin insulation regular placing layer process between layers which forms a circuit can be performed. in addition, the thing for which this resin insulation regular placing layer process between layers is repeated two or more times in the manufacture approach of this invention depending on IC chip mounting substrate to manufacture although this resin insulation regular placing layer process between layers was performed only once — the resin insulating layer between layers, and a conductor — it is good also as a gestalt by which every laminating formation of the circuit was carried out more than two-layer.

[0065] (C) Next, perform the solder resist layer formation process (C) which forms a solder resist layer in the outermost layer. After applying a non-hardened solder resist constituent by the roll coater, curtain coater, etc. or specifically sticking by pressure the solder resist constituent fabricated in the shape of a film, a solder resist

layer is formed by performing hardening processing.
[0066] The above-mentioned solder resist layer is [0067] which can be formed using the solder resist constituent containing for example, polyphenylene ether resin, polyolefin resin, a fluororesin, thermoplastic elastomer, an epoxy resin, polyimide resin, etc. moreover, as solder resist constituents other than the above For example, the acrylate (meta) of a novolak mold epoxy resin, an imidazole curing agent, 2 functionality (meta) acrylic ester monomer, the polymer of with a molecular weight of about 500 to 5000 acrylic ester (meta), The fluid of the shape of a paste containing photosensitive monomers, such as thermosetting resin which consists of a bisphenol mold epoxy resin etc., and a multiple-valued acrylic monomer, a glycol ether system solvent, etc. is mentioned, and, as for the viscosity, it is desirable to be adjusted to 1 - 10 Pa-s at 25 degrees C. Moreover, as for the above-mentioned solder resist constituent, the elastomer and the inorganic filler may be blended. Moreover, a commercial solder resist constituent may be used as a solder resist constituent.
[0068] Moreover, opening for solder bump formation is formed in the above-mentioned solder resist layer by the lasing or the exposure development if needed. Under the present circumstances, the same thing as the laser used in case opening for the Bahia halls mentioned above is formed as laser to be used etc. is **********.
[0069] next, the conductor exposed to the base of the above-mentioned opening for solder bump formation — a metal layer is formed on the surface of a circuit if needed. the above-mentioned metal layer — corrosion-resistant metals, such as nickel, palladium, gold, silver, and platinum, — the above — a conductor — it can form by covering a circuit front face. Specifically, it is desirable to form with metals, such as nickel-gold, nickel-silver, nickel-palladium, and nickel-palladium-gold. Moreover, although the above-mentioned solder pad can be formed using approaches, such as plating, vacuum evaporationo, and electrodeposition, in these, the point of excelling in the homogeneity of an enveloping layer to its plating is desirable. Moreover, the mark for alignment used at the process mentioned later in the case of lamination with the substrate for optical element insertion may be formed in the solder resist layer formed at this process. Such (A) A package substrate is producible by passing through the process of - (C).
[0070] next, pass the process of above-mentioned (a) - (c) — pass the process of the produced substrate for optical element insertion, and above-mentioned (A) - (C) — pass the process of following (1) - (3) after sticking the produced package substrate through the adhesives layer which the substrate for optical element insertion has — how to use as the substrate for IC chip mounting is explained.
[0071] Lamination of the substrate for optical element insertion and a package substrate can be performed using for example, a pin lamination method, a mass lamination method, etc. After performing both alignment, specifically, the substrate for optical element insertion and a package substrate are stuck by carrying out a temperature up to the temperature (usually about 60-200 degrees C) which an adhesives layer softens, and subsequently pressing by the pressure of 1 - 10MPa extent.
[0072] (1) the conductor of the above-mentioned optical element after attaching an optical element in the front face of the package substrate first exposed from the through tube formed in the above-mentioned substrate for optical element insertion, and the above-mentioned package substrate — perform the optical element mounting process (1) of connecting a circuit electrically.
[0073] As an optical element mounted at this process, light emitting devices, such as photo detectors, such as PD (photodiode) and APD (avalanche photodiode), LD (semiconductor laser), DFB-LD (distribution feedback mold-semiconductor laser), and LED (light emitting diode), etc. are **********, for example.
[0074] As an ingredient of the above-mentioned photo detector, Si, germanium, InGaAs, etc. are mentioned, for example. In these, a point to InGaAs which is excellent in light-receiving sensibility is desirable. Moreover, as an ingredient of the above-mentioned light emitting device, a gallium, arsenic and the compound (GaAsP) of Lynn, a gallium, aluminum and the compound (GaAlAs) of arsenic, a gallium and the compound (GaAs) of arsenic, an indium, a gallium and the compound (InGaAs) of arsenic, an indium, a gallium, arsenic, the compound (InGaAsP) of Lynn, etc. are mentioned, for example. That what is necessary is just to use these properly in consideration of communication link wavelength, when communication link wavelength is 0.85-micrometer band, GaAlAs can be used, and in the case of 1.3-micrometer band or 1.55-micrometer band, communication link wavelength can use InGaAs and InGaAsP.
[0075] After installation of the above-mentioned optical element prepares the solder resist layer which has opening in the rear face of an optical element, attaches adhesives in opening and lays them in a package substrate, it is desirable to carry out by the reflow. Especially the thing for which a dummy pad is prepared in the bottom of opening of the solder resist layer by the side of the substrate for IC chip mounting, and a reflow is performed especially is desirable. It is desirable to carry out by die bonding, using solder (low-melt point point metal) pastes, such as Sn/Pb and Sn/Ag, and the die bond resin for various adhesion as adhesives. It is because an optical element can be attached in a desired location by the self-alignment in the case of die bonding. Not using Pb, a SnAg system and a SnAgCu system are good as solder from a wettability point. What is necessary is

just to perform temperature of a reflow in the range of 10-50 degrees C of melting point pluses of solder. It dissolves by the reflow and also solder may be dissolved in oven.

[0076] It can carry out by for example, the eutectic joining-together method, the solder joining-together method, a resin bond method, etc. besides die bonding. In these, workability is good and a resin bond method is economically desirable at an advantageous point. By the describing [above] resin bond method, thermosetting resin, such as epoxy system resin and polyimide system resin, is used as base resin, the paste which contains a curing agent, a filler, a solvent, etc. in addition to these resinous principles is applied on a package substrate, and subsequently to a paste top, after laying an optical element, an optical element is attached by carrying out heat hardening of this paste. In addition, spreading of the above-mentioned paste can be performed with for example, the dispensing method, the **********ing method, screen printing, etc.

[0077] the conductor of the above-mentioned optical element and the above-mentioned package substrate — as an approach of connecting a circuit electrically, it is desirable to use wirebonding. It is because it is economically advantageous while this has the large degree of freedom of the design at the time of attaching an optical element. As the above-mentioned wirebonding, a well-known approach, i.e., the nail-head-bonding method and the wedge bonding method, can be used conventionally. In addition, connection between an optical element and a package substrate may be made by tape automated bonding, flip chip bonding, etc.

[0078] (2) Next, perform the solder resist layer formation process which forms a solder resist layer in the exposure of the above-mentioned substrate for optical element insertion. At this process, after applying a non-hardened solder resist constituent by the roll coater, curtain coater, etc. or specifically sticking by pressure the solder resist constituent fabricated in the shape of a film, a solder resist layer is formed by performing hardening processing. The same thing as the solder resist constituent used as the above-mentioned solder resist constituent, for example when producing a package substrate etc. can be used.

[0079] Moreover, since the solder resist layer is already formed before performing this process, it is not necessary to form a solder resist layer in the exposure of a package substrate at this process.

[0080] Moreover, alignment is carried out to the above-mentioned solder resist layer on the basis of an optical element, and opening for solder bump formation is formed in it by the lasing or the exposure development. Under the present circumstances, the same thing as the laser used in case opening for the Bahia halls mentioned above is formed as laser to be used etc. is mentioned.

[0081] (3) Next, it is filled up with a resin constituent in the through tube formed in the above-mentioned substrate for optical element insertion, and perform the resin packed bed formation process which forms a resin packed bed. What uses as a resinous principle thermosetting resin, thermoplastics, a photopolymer, the resin with which some thermosetting resin was photosensitivity-ized, these complex, etc. as the above-mentioned resin constituent is mentioned. As an example of the above-mentioned resinous principle, an epoxy resin, phenol resin, polyimide resin, olefine resin, BT resin, etc. are mentioned, for example. Moreover, particles, such as for example, a resin particle, an inorganic particle, and metal particles, may be contained in the above-mentioned resin constituent in addition to the above-mentioned resinous principle. By including these particles, adjustment of a coefficient of thermal expansion can be aimed at between a resin packed bed, a substrate and a solder resist layer, the resin insulating layer between layers, etc., and fire retardancy can also be given depending on the class of particle.

[0082] As the above-mentioned resin particle, the resin complex of thermosetting resin, thermoplastics, a photopolymer, the resin with which some thermosetting resin was photosensitivity-ized, thermosetting resin, and thermoplastics, the complex of a photopolymer and thermoplastics, etc. are mentioned, for example.

[0083] Specifically For example, an epoxy resin, phenol resin, polyimide resin, Thermosetting resin, such as a bismaleimide resin, polyphenylene resin, polyolefin resin, and a fluororesin; The heat-curing radical of these thermosetting resin A methacrylic acid, an acrylic acid, etc. are made to react to (for example, the epoxy group in an epoxy resin). Resin which gave the acrylic radical; Phenoxy resin, polyether sulfone (PES), Thermoplastics, such as polysulfone (PSF), a polyphenylene sulfone (PPS), polyphenylene sulfide (PPES), a polyphenyl ether (PPE), and polyether imide (PI); photopolymers, such as acrylic resin, etc. are mentioned. Moreover, the resin complex of the resin complex of the above-mentioned thermosetting resin and the above-mentioned thermoplastics, the resin which gave the above-mentioned acrylic radical, the above-mentioned photopolymer, and the above-mentioned thermoplastics can also be used. Moreover, the resin particle which consists of rubber can also be used as the above-mentioned resin particle.

[0084] Moreover, as the above-mentioned inorganic particle, silicon compounds, such as magnesium compounds, such as potassium compounds, such as lime compounds, such as aluminium compounds, such as an alumina and an aluminum hydroxide, a calcium carbonate, and a calcium hydroxide, and potassium carbonate, a magnesia, a dolomite, and basic magnesium carbonate, a silica, and a zeolite, etc. are mentioned, for example. Moreover, what consists of Lynn or phosphorus compounds can also be used as the above-mentioned inorganic particle.

[0085] As the above-mentioned metal particles, Au, Ag, Cu, Pd, nickel, Pt, Fe, Zn, Pb, aluminum, Mg, calcium, etc. are mentioned, for example. These resin particles, an inorganic particle, and metal particles may be used independently, respectively, and may be used together two or more sorts.
[0086] Moreover, especially the configuration of the above-mentioned particle is not limited, for example, the shape of a globular shape, an ellipse globular shape, the letter of crushing, and a polyhedron etc. is mentioned. Moreover, as for the particle size (the die length of the longest part of a particle) of the above-mentioned particle, it is desirable that it is shorter than the wavelength of communication link light. It is because transmission of a lightwave signal may be checked when particle size is longer than the wavelength of communication link light.
[0087] It is not limited especially as an approach filled up with the above-mentioned resin constituent, for example, approaches, such as printing and potting, can be used. Moreover, it may be filled up with what was made into the shape of a tablet using a plunger. Moreover, after being filled up with a resin packed bed, hardening processing etc. is performed if needed.
[0088] Moreover, as for the resin packed bed formed at this process, it is desirable for the permeability of the communication link wavelength light of that perpendicular direction to be 90% or more. It is because un-arranging may occur in the communication link of the lightwave signal with which transmission of communication link light was checked and the above-mentioned permeability minded the optical element at less than 90%. In addition, in this specification, the permeability (%) of communication link wavelength light is a value computed from the following formula (1), when the intensity of light which passed I1 and the above-mentioned resin packed bed, and came out of the strength of the incident light of the perpendicular direction to the above-mentioned resin packed bed is set to I2.
[0089]
Permeability (%) =(I2/I1) x100 ... (1)
[0090] Moreover, in case a resin constituent is filled up with this process, multiple times may be divided and filled up with a different resin constituent, and the resin layer which consists of two or more layers may be formed in a through tube. It is filling up the field to the height of the light-receiving side of a photo detector, or the luminescence side of a light emitting device with the resin constituent excellent in the property protecting wirebonding, its connection area, etc., and the resin constituent excellent in especially thermal resistance, and specifically forming a resin packed bed especially in a field higher than the above-mentioned light-receiving side and a luminescence side using the resin constituent which is excellent in the transmission nature of communication link light etc.
[0091] Furthermore, it is desirable to perform polish processing to the exposure of the resin constituent exposed from the through tube at this process, and to make that exposure flat. By making an exposure flat, it is because a possibility that transmission of communication link light may be checked decreases more. Polish by buffing, a sandpaper, etc., mirror polishing, clean polish, etc. can perform the above-mentioned polish processing. Moreover, chemical polishing using an acid, an oxidizer, a drug solution, etc. may be performed. Moreover, two or more sorts of polish processings may be performed combining these approaches.
[0092] Moreover, after forming the above-mentioned resin packed bed, the through hole which penetrates the above-mentioned substrate for optical element insertion and the above-mentioned package substrate may be formed if needed. Specifically, the through tube for through holes which penetrates the above-mentioned substrate for optical element insertion and the above-mentioned package substrate is first formed by drilling, the lasing, etc. Next, a thin film conductor layer is formed in the exposure of the substrate for optical element insertion containing the wall surface of this through tube for through holes, and the exposure of a BAKKEJI substrate by nonelectrolytic plating, sputtering, etc. Furthermore, after forming plating resist on the substrate with which the thin film conductor layer was formed in the front face, the through hole which penetrates the above-mentioned substrate for optical element insertion and the above-mentioned package substrate can be formed by forming an electrolysis plating layer in this plating-resist agenesis section, and removing the thin film conductor layer under the above-mentioned plating resist and this plating resist after that.
[0093] Moreover, after replacing with the approach of forming an electrolysis plating layer after forming plating resist which was mentioned above and forming an electrolysis plating layer the whole surface on a thin film conductor layer, etching resist and a solder plating layer are formed on an electrolysis plating layer, and even if it uses the approach of giving etching processing further, the through hole penetrate the above-mentioned substrate for optical element insertion and the above-mentioned package substrate can be formed. In addition, after forming a through hole, it is desirable to be filled up with a resin filler in this through hole.
[0094] next, the conductor exposed to the base of the above-mentioned opening for solder bump formation — a metal layer is formed on the surface of a circuit if needed. the above-mentioned metal layer — corrosion-resistant metals, such as nickel, palladium, gold, silver, and platinum, — the above — a conductor — it can form

by covering a circuit front face. Specifically, it is desirable to form with metals, such as nickel-gold, nickel-silver, nickel-palladium, and nickel-palladium-gold. Moreover, although the above-mentioned metal layer can be formed using approaches, such as plating, vacuum evaporationo, and electrodeposition, in these, the point of excelling in the homogeneity of an enveloping layer to its plating is desirable. In addition, in case this metal layer forms a solder bump etc. at a back process, it will play a role of a solder pad.

[0095] Furthermore, after filling up the above-mentioned opening for solder bump formation with soldering paste through the mask with which opening was formed in the part equivalent to the above-mentioned opening for solder bump formation if needed, a solder bump is formed by carrying out a reflow. The substrate for IC chip mounting can be manufactured by passing through such a series of processes.

[0096]

[Example] First, the configuration of the substrate 20 for IC chip mounting concerning the 1st example of this invention is explained with reference to drawing 11 and drawing 12 . Drawing 11 is the fragmentary sectional view showing typically some substrates for IC chip mounting concerning the 1st example, and drawing 12 is the fragmentary sectional view showing typically the condition of having carried IC chip in the substrate for IC chip mounting shown in drawing 11 , and having attached in the DOTA board.

[0097] As shown in drawing 11 , the substrate 20 for IC chip mounting consists of the package substrate 10 which consists of a multilayer build up patchboard carrying IC chip, and the substrate 100 for optical element insertion equipped with the through-hole 98 which holds a light emitting device 12 and a photo detector 14. In the through-hole 98, the resin packed bed 74 with which it comes to fill up resin equipped with translucency is formed.

[0098] the package substrate 10 — both sides of the core substrate 30 — a conductor — the resin insulating layer 50 between layers in which the circuit 60 and the Bahia hall 58 were formed, and a conductor — the resin insulating layer 150 between layers in which the circuit 160 and the Bahia hall 158 were formed is formed, and it changes. a through hole 36 forms in the core substrate 30 — having — both sides of the core substrate 30 — a conductor — the circuit 38 is formed. The solder resist layer 62 is arranged on the resin insulating layer 150 between layers. Solder bump 79D for connection with IC chip is arranged at opening 62a by the side of the inferior surface of tongue in drawing of the solder resist layer 62 (IC tip side), and the wire 72 from a light emitting device 12 and a photo detector 14 is connected to the pad 69 in opening 62a by the side of a top face.

[0099] The substrate 100 for optical element insertion consists of a core substrate 80 with which the through-hole 98 was formed. The through hole 86 is formed in this core substrate 80. land 86a by the side of drawing Nakashita of this through hole 86 — the conductor of the package substrate 10 — it connects with a circuit 160 and the lid plating layer 94 is arranged in land 86b by the side of drawing Nakagami. The solder resist layer 76 is formed in this lid plating layer 94 bottom, and solder bump 79U linked to a DOTA board is formed on the lid plating layer 94 through opening 76a of the solder resist layer 76.

[0100] As shown in drawing 12 , the IC chip 102 is connected to the substrate 20 for IC chip mounting through solder bump (or BGA) 79D. On the other hand, the substrate 20 for IC chip mounting is connected to the DOTA board 108 through solder bump 79U. Optical waveguide (or optical fiber) 16 and optical waveguide (or optical fiber) 18 are horizontally arranged by the DOTA board 108. End-face 16a of optical waveguide 16 and end-face 18a of optical waveguide 18 are cut into 45 degrees.

[0101] The lightwave signal which penetrates optical waveguide 16 is sent upwards through end-face 16a cut into 45 degrees, and incidence is carried out to light sensing portion 14a of a photo detector 14. the lightwave signal by which incidence was carried out is changed into a photo detector 14 at an electrical signal — having — the conductor in the package substrate 10 — it is transmitted to the IC chip 102 through a circuit. namely, the conductor of the resin insulating layer 150 between layers by the side of a photo detector 14-wire 72-photo detector — the conductor of a circuit 160 and the resin insulating layer 50 between layers by the side of a Bahia hall 158-photo detector — the conductor of a circuit 60 and the resin insulating layer 50 between layers of the Bahia hall 58-through hole 36-IC tip side — the conductor of a circuit 60 and the resin insulating layer 150 between layers of the Bahia hall 58-IC tip side — it is the circuit 160 and Bahia hall 158-solder bump (or BGA) 76 U-IC chip 102.

[0102] The result of an operation in the IC chip 102 based on the lightwave signal from the above-mentioned photo detector 14 is sent to the DOTA board 108 through the package substrate 10 and the substrate 100 for optical element insertion. that is IC chip 102-solder bump () or the conductor of the resin insulating layer 150 between layers of the BGA76 U-IC tip side — the conductor of a circuit 160 and the resin insulating layer 50 between layers of the Bahia hall 158-IC tip side — the conductor of a circuit 60 and the resin insulating layer 50 between layers by the side of a Bahia hall 58-through hole 36-DOTA board — a circuit 60 — the conductor of the resin insulating layer 150 between layers by the side of a Bahia hall 58-DOTA board — it is through hole 86-solder bump 79U of a circuit 160 and the substrate 100 for Bahia hall 158-optical element insertion.

[0103] On the other hand, the command from the DOTA board 108 side is sent to the IC chip 102 through the substrate 100 for optical element insertion, and the package substrate 10. that is the conductor of the resin insulating layer 150 between layers by the side of the through hole 86-DOTA board of the substrate 100 for solder bump 79U-optical element insertion — a circuit 160 — the conductor of the resin insulating layer 50 between layers by the side of a Bahia hall 158-DOTA board — the conductor of a circuit 60 and the resin insulating layer 50 between layers of the Bahia hall 58-through hole 36-IC tip side — the conductor of a circuit 60 and the resin insulating layer 150 between layers of the Bahia hall 58-IC tip side — a circuit 160 — It is the Bahia hall 158-solder bump (or BGA) 76 U-IC chip 102.
[0104] The electrical signal from the IC chip 102 is transmitted to a light emitting device 12 through the package substrate 10. namely, the conductor of the resin insulating layer 150 between layers of the IC chip 102-solder bump (or BGA) 76 U-IC tip side — the conductor of a circuit 160 and the resin insulating layer 50 between layers of the Bahia hall 158-IC tip side — the conductor of a circuit 60 and the resin insulating layer 50 between layers by the side of a Bahia hall 58-through hole 36-DOTA board — the conductor of a circuit 60 and the resin insulating layer 150 between layers by the side of a Bahia hall 58-DOTA board — it is the circuit 160-wire 72-light emitting device 12. It is changed into a lightwave signal by the light emitting device 12, and is perpendicularly discharged from light-emitting part 12a to the method of drawing Nakashita, and incidence of the electrical signal is carried out through end-face 18a cut into 45 degrees, and it penetrates the inside of optical waveguide 18.
[0105] Drawing 15 is the top view of the substrate 20 for IC chip mounting shown in drawing 11 . the conductor which mainly connects a light emitting device 12 and the IC chip 102 to the loading side L of the light emitting device 12 of the package substrate (multilayer printed wiring board) 10 — the circuit (conductor a circuit 60, the Bahia hall 58, a conductor a circuit 160, the Bahia hall 158) is arranged. For this reason, the output terminal (pad) 104 by the side of the light emitting device 12 of the IC chip 102 is designed so that it may mainly come to the loading side [a light emitting device 12] L side.
[0106] the conductor which, on the other hand, mainly connects a photo detector 14 and the IC chip 102 to the loading the photo detector 14 of the package substrate (multilayer printed wiring board) 10 side R — the circuit (conductor a circuit 60, the Bahia hall 58, a conductor a circuit 160, the Bahia hall 158) is arranged. For this reason, the input terminal (pad) 104 from the photo detector 14 of the IC chip 102 is designed so that it may mainly come to the loading side [a photo detector 14] R side.
[0107] the conductor which mainly connects a light emitting device 12 and the IC chip 102 to the light emitting device loading side L in the 1st example as mentioned above — the conductor which arranges a circuit and mainly connects a photo detector 14 and the IC chip 102 to the photo detector loading side R — a circuit is arranged. for this reason, the conductor which connects a photo detector 14 and the IC chip 102 — the conductor which connects the die length, and a light emitting device 12 and the IC chip 102 of a circuit — the die length of a circuit becomes short and a photo detector 14, a light emitting device 12, and IC chip can be connected rationally. moreover, the conductor which transmits the input from a photo detector 14 — the conductor which delivers a circuit the output to a light emitting device 12 — effect of a noise etc. can be made hard to separate I/O and to affect it, in order to divide and arrange a circuit within a multilayer printed wiring board.
[0108] moreover, the conductor which connects the IC chip 102, a photo detector 14, and a light emitting device 12 in the 1st example — the conductor which a circuit is arranged mainly in the center section and, on the other hand, ties the IC chip 102 and the DOTA board 108 — the circuit is arranged mainly in the periphery section. Here between the IC chip 102, a photo detector 14, and a light emitting device 12 The signal of a high frequency is sent and received relatively. Between the IC chip 102 and the DOTA board 108 the conductor between the IC chip 102 with which the signal of a high frequency is sent and received since the signal of a low frequency is sent and received relatively, a photo detector 14, and a light emitting device 12 — the die length of a circuit is shortened and the RF engine performance of the substrate for IC chip mounting is improved.
[0109] Hereafter, the production process of the substrate 20 for IC chip mounting mentioned above with reference to drawing 11 is explained with reference to drawing 1 - drawing 13 .
[0110] A. the preparation bisphenol female mold epoxy monomer (oil-ized shell company make —) of (Production a) resin filler of the substrate for optical element insertion The mean particle diameter by which coating of the silane coupling agent was carried out to 310, the YL983U100 weight section, and a front face Molecular weight : by 1.6 micrometers The diameter of grain of maximum size for a container the SiO2 spherical-particle (Adtec Corp. make, CRS 1101-CE) 72 weight section 15 micrometers or less and the leveling agent (Sannopuko beret Norian S4) 1.5 weight section by carrying out stirring mixing The viscosity prepared the resin filler of 30-60Pa and s at 23**1 degree C. In addition, the imidazole curing agent (Shikoku formation shrine make, 2E4 MZ-CN) 6.5 weight section was used as a curing agent.

[0111] (b) Double-sided copper clad laminate 80A which 18-micrometer copper foil 81 laminates on one side of the insulating substrate 80 which consists of the glass epoxy resin with a manufacture (1) thickness of 0.8mm or BT (bismaleimide triazine) resin of the substrate for optical element insertion was used as the start ingredient (refer to drawing 1 (A)). First, the conductor layer 82 was formed in that front face (the wall surface of a through tube 84 is included) by drilling a through tube 84 in this copper clad laminate with a drill, and performing nonelectrolytic plating processing (refer to drawing 1 (B)).
[0112] (2) Next, after washing in cold water the substrate 1 in which the conductor layer 82 was formed and drying, Melanism processing the water solution containing NaOH (10g/(l.)), NaClO2 (40 g/l), and Na3PO4 (6 g/l) -- melanism -- it considers as a bath (oxidation bath) -- And reduction processing which makes a reduction bath NaOH (10 g/l) and the water solution containing NaBH4 (6g/(l.)) was performed, and roughening side 82alpha was formed in the front face of a conductor layer 82 (refer to drawing 1 (C)).
[0113] (3) After preparing the resin filler indicated above (a) below, it was filled up with the resin filler 90 in the through tube 84 which formed the conductor layer 82 in the wall surface within 24 hours after adjustment by the following approach (drawing 1 (D)). That is, after pushing in a resin filler in a through tube using a squeegee, it was made to dry on 100 degrees C and the conditions for 20 minutes.
[0114] (4) By belt sander polish using the belt abrasive paper (Sankyo Rikagaku make) of **600, one side of a substrate which finished processing of the above (3) was ground so that the exposure of the layer of the resin filler 90 and the front face of a conductor layer 82 might become flat, and subsequently buffing for removing the blemish by the above-mentioned belt sander polish was performed. Such a series of polishes were similarly performed about the field of another side of a substrate. Subsequently, by 100 degrees C, it performed at 150 degrees C for 1 hour for 3 hours, 120 degrees C performed heat-treatment of 7 hours at 180 degrees C for 1 hour, and the resin filler layer 90 was formed (refer to drawing 1 (E)).
[0115] (5) Next, the conductor layer 92 was formed by performing nonelectrolytic plating processing to one side of the substrate in which the conductor layer 82 was formed (refer to drawing 2 (A)). In addition, the conductor layer 92 was beforehand formed in the field of the example which gives the palladium catalyst and does not form a conductor layer 92 by forming plating resist in the field which forms a conductor layer 92 at one side of a substrate.
[0116] (6) the conductor of the substrate in which the conductor layer 82 and the conductor layer 92 were formed -- by performing etching processing, after forming etching resist (not shown) in the part equivalent to the circuit (land part of through hole is included) formation section the through hole 86 where the resin filler layer 90 was formed in the interior, and the lid plating layer 94 was formed in the upper part, and a conductor -- a circuit (not shown) -- forming -- the lid plating layer 94 and a conductor -- roughening layer 94alpha was prepared on the surface of the circuit (refer to drawing 2 (B)).
[0117] In addition, formation of etching resist stuck the commercial photosensitive dry film, laid the mask, exposed it by 100 mJ/cm2, and was performed by carrying out a development in a sodium-carbonate water solution 0.8%. Moreover, etching processing was performed using the mixed liquor of a sulfuric acid and a hydrogen peroxide.
[0118] (7) next, the conductor of one side of a substrate 80 -- the adhesives layer 96 was formed by applying epoxy resin adhesive to the circuit agenesis section (refer to drawing 2 (C)).
[0119] (8) Further, in the center section of a substrate 80, by router processing, the through tube 98 for optical element hold was formed, and it considered as the substrate 100 for optical element insertion (refer to drawing 2 (D)).
[0120] B. The production bisphenol A mold epoxy resin (weight-per-epoxy-equivalent 469, Epicoat 1001 by oil-ized shell epoxy company) 30 weight section of the resin film for the resin insulating layers between the (production a) layers, [of a package substrate] The cresol novolak mold epoxy resin (weight-per-epoxy-equivalent 215, Epiclon N-673 by Dainippon Ink & Chemicals, Inc.) 40 weight section, The triazine structure content phenol novolak resin (phenol nature hydroxyl equivalent 120, Dainippon Ink & Chemicals, Inc. make FENO light KA-7052) 30 weight section The ethyl diethylene glycol acetate 20 weight section, The heating dissolution is carried out stirring in the solvent naphtha 20 weight section. There The end epoxidation polybutadiene rubber (Nagase Brothers formation DENAREKKUSU R-45 by industrial company EPT) 15 weight section, and the 2-phenyl -4, the 5-screw (hydroxymethyl) imidazole grinding article 1.5 weight section, The pulverizing silica 2 weight section and the silicon system defoaming agent 0.5 weight section were added, and the epoxy resin constituent was prepared. After applying using a roll coater so that the thickness after drying the obtained epoxy resin constituent on a PET film with a thickness of 38 micrometers may be set to 50 micrometers, the resin film for the resin insulating layers between layers was produced by making it dry for 10 minutes at 80-120 degrees C.

[0121] (b) It carried out like the process of (a) of production of the substrate for adjustment optical element

insertion of a resin filler.
[0122] (e) Double-sided copper clad laminate 30A which 18-micrometer copper foil 32 laminates to both sides of the insulating substrate 30 which consists of the glass epoxy resin with a manufacture (1) thickness of 0.8mm or BT (bismaleimide triazine) resin of a package substrate was used as the start ingredient (refer to drawing 3 (A)). First, the through tube 34 was drilled in this copper clad laminate with the drill, nonelectrolytic plating processing was performed, and the conductor layer 33 was formed (refer to drawing 3 (B)). and the thing to etch in the shape of a pattern — both sides of a substrate 30 — a lower layer — a conductor — the circuit 38 and the through hole 36 were formed (refer to drawing 3 (C)).
[0123] (2) a lower layer — a conductor — washing in cold water the substrate 30 in which the circuit 38 was formed, and, after drying Melanism processing the water solution containing NaOH (10g/(l.)), NaClO2 (40 g/l), and Na3PO4 (6 g/l) — melanism — it considers as a bath (oxidation bath) — and the reduction processing which makes a reduction bath NaOH (10 g/l) and the water solution containing NaBH4 (6 g/l) — carrying out — a lower layer — a conductor — the roughening sides 38alpha and 36alpha were formed in the front face of a circuit 38, and the inside of a through hole 36 (refer to drawing 3 (D)).
[0124] (3) the following approach after preparing the resin filler indicated above (b) below — after adjustment — less than 24 hours — the conductor of one side of the inside of a through hole 36, and a substrate 30 — the circuit agenesis section and a lower layer — a conductor — the layer of the resin filler 40 was formed in the rim section of a circuit 38 (refer to drawing 3 (E)). That is, after pushing in the resin filler 40 in a through hole 36 using a squeegee, it was made to dry on 100 degrees C and the conditions for 20 minutes first. next, a conductor — the conductor with which the part equivalent to the circuit agenesis section lays on a substrate the mask which carried out opening, and serves as a crevice using the squeegee — the circuit agenesis section was also filled up with the resin filler 40, and the layer of the resin filler 40 was formed by making it dry on 100 degrees C and the conditions for 20 minutes.
[0125] (4) the belt sander [one side / which finished processing of the above (3) / of a substrate] polish using the belt abrasive paper (Sankyo Rikagaku make) of **600 — a conductor — it ground so that the resin filler 40 might remain neither in the front face of a circuit 38, nor the land front face of a through hole 36, and subsequently buffing for removing the blemish by the above-mentioned belt sander polish was performed. Such a series of processings were similarly performed about the field of another side of a substrate. Subsequently, by 100 degrees C, it performed at 150 degrees C for 1 hour for 3 hours, 120 degrees C performed heat-treatment of 7 hours at 180 degrees C for 1 hour, and the resin filler layer 40 was formed (refer to drawing 4 (A)).
[0126] thus, a through hole 36 and a conductor — the surface section of the resin filler layer 40 formed in the circuit agenesis section, and a conductor — the front face of a circuit 38 — flattening — carrying out — the resin filler layer 40 and a conductor — the insulating substrate which the side face of a circuit 38 stuck firmly through roughening side 38alpha, and the internal surface and the resin filler layer 40 of a through hole 36 stuck firmly through roughening side 36alpha was obtained. this process — the front face of the resin filler layer 40, and a conductor — the front face of a circuit 38 turns into the same flat surface.
[0127] (5) software etching after rinsing and carrying out acid cleaning of the above-mentioned substrate — carrying out — subsequently — an etching reagent — both sides of a substrate — a spray — spraying — a conductor — etching the front face of a circuit 38, and the land front face of a through hole 36 — a conductor — all the front faces of a circuit 38 — roughening side 38beta — moreover, roughening side 36beta was formed in the land of a through hole 36 (drawing 4 (B)). As an etching reagent, the etching reagent (the product made from MEKKU, MEKKU dirty bond) containing the imidazole copper (II) complex 10 weight section, the glycolic-acid 7 weight section, and the potassium chloride 5 weight section was used.
[0128] (6) Next, by 0.5MPa, it laminated vaccum pressure arrival, the resin film for the resin insulating layers between layers produced above (a) was stuck, carrying out a temperature up to the temperature of 50-150 degrees C, and 50gamma of resin film layers was formed (refer to drawing 4 (C)).
[0129] (7) Next, through the mask with which the through tube with a thickness of 1.2mm was formed on 50gamma of resin film layers, on the beam diameter of 4.0mm, the Top Hat mode, 8.0 microseconds of pulse width, the path of 1.0mm of the through tube of a mask, and the conditions of one shot, opening 50a for the with a diameter of 80 micrometers Bahia halls be formed in 50gamma of resin film layers, and it considered as the resin insulating layer 50 between layers in CO2 gas laser with a wavelength of 10.4 micrometers (refer to drawing 4 (D)).
[0130] (8) Roughening side 50alpha was formed in the front face of the resin insulating layer 50 between layers containing the internal surface of opening 50a for the Bahia halls by immersing the substrate in which opening 50a for the Bahia halls was formed, for 10 minutes in the 80-degree C solution containing the permanganic acid of 60 g/l, and carrying out dissolution removal of the epoxy resin particle which exists in the front face of the resin insulating layer 50 between layers (drawing 4 (E)).

[0131] (9) Next, the substrate which finished the above-mentioned processing was washed in cold water after being immersed in the neutralization solution (product made from SHIPUREI). Furthermore, the catalyst nucleus was made for the front face of this substrate that carried out the surface roughening process (a roughening depth of 3 micrometers) to adhere to the front face (for the internal surface of opening 50a for the Bahia halls to be included) of the resin insulating layer 50 between layers by giving a palladium catalyst (not shown). That is, the above-mentioned substrate was immersed into the catalytic liquid containing a palladium chloride (PbCl2) and a stannous chloride (SnCl2), and the catalyst was given by depositing a palladium metal.
[0132] (10) Next, into the non-electrolytic copper plating liquid of the following presentations, the substrate was immersed and the non-electrolytic copper plating film (thin film conductor layer) 52 with a thickness of 0.6-3.0 micrometers was formed on the front face (the internal surface of opening 50a for the Bahia halls is included) of the resin insulating layer 50 between layers (refer to drawing 5 (A)).
[Nonelectrolytic plating liquid]
NiSO4 0.003 mol/l tartaric acid 0.200 mol/l copper sulfate 0.030 mol/lHCHO 0.050 mol/lNaOH 0.100 mol/lalpha, alpha' - BIBIRIJIRU 100 mg/l Polyethylene glycol (PEG) 0.10 g/l [Nonelectrolytic plating conditions]
It is 40 minutes [0133] by whenever [34-degree C solution temperature]. (11) Next, plating resist 54 was formed by sticking a commercial photosensitive dry film on the substrate with which the non-electrolytic copper plating film 33 was formed, laying a mask, exposing by 100 mJ/cm2, and carrying out a development in a sodium-carbonate water solution 0.8% (refer to drawing 5 (B)).
[0134] (12) Subsequently, 50-degree C water washed the substrate and it degreased, with 25-degree C water, after washing with the sulfuric acid further after rinsing, electrolysis plating was performed on condition that the following, and the electrolytic copper plating film 56 was formed in the plating-resist 54 agenesis section (refer to drawing 5 R> 5 (C)).
[Electrolysis plating liquid]
Sulfuric acid 2.24 mol/l copper sulfate 0.26 mol/l additive 19.5 ml/l (made in ATOTEKKU Japan, hippo RASHIDO GL)
[Electrolysis plating conditions]
Current density 1 A/dm 2 hours 65 Part temperature 22**2 ** [0135] (13) — the nonelectrolytic plating film under the plating resist 54 after carrying out exfoliation removal of the plating resist 54 by KOH 5% further — the mixed liquor of a sulfuric acid and a hydrogen peroxide — etching processing — carrying out — dissolution removal — carrying out — the upper layer — a conductor — it considered as the circuit 60 (the Bahia hall 58 is included) (refer to drawing 5 (D)).
[0136] (14) next, the upper layer — a conductor — the substrate 30 in which the circuit 60 grade was formed — an etching reagent — being immersed — the upper layer — a conductor — the roughening sides 60alpha and 58alpha were formed in the front face of a circuit 60 (the Bahia hall 58 is included) (refer to drawing 6 (A)). In addition, as an etching reagent, the product made from MEKKU and MEKKU dirty bond were used.
[0137] (15) Then, form the resin insulating layer 150 between layers in the upper layer further by repeating the process of above-mentioned (6) - (15). and the resin insulating-layer 150 top between layers — a conductor — dummy pad (conductor circuit) 160c for fixing a circuit 160 (the Bahia hall 158 being included) and a photo detector, and a light emitting device is formed (drawing 6 (B)).
[0138] (16) Next, made it dissolve so that it may become 60% of the weight of concentration to diethylene-glycol wood ether (DMDG). The oligomer (molecular weight: 4000) 46.67 weight section of the photosensitive grant which acrylic-ized 50% of epoxy groups of a cresol novolak mold epoxy resin (Nippon Kayaku Co., Ltd. make), 80% of the weight of the bisphenol A mold epoxy resin (oil-ized shell company make —) dissolved in the methyl ethyl ketone trade name: — the Epicoat 1001 15.0 weight section and an imidazole curing agent (Shikoku — formation — shrine make —) trade name: — 2 organic-functions acrylic monomer (the Nippon Kayaku Co., Ltd. make —) which are the 2E4 MZ-CN1.6 weight section and a photosensitive monomer trade name: — the R604 4.5 weight section — the same — a multiple-valued acrylic monomer (the Kyoei Kagaku K.K. make —) trade name: — the DPE6A1.5 weight section and a dispersed system defoaming agent (the Sannopuko make —) Stir the S-65 0.71 weight section for a container, mix, and a mixed constituent is prepared. The solder resist constituent which adjusted viscosity to 2.0 Pa-s at 25 degrees C was obtained by adding the benzophenone (Kanto chemistry company make) 2.0 weight section and the Michler's-ketone (Kanto chemistry company make) 0.2 weight section as a photosensitizer as a photopolymerization initiator to this mixed constituent. Moreover, in the case of 60rpm, in the case of rotor No.4 and 6rpm, measurement of viscosity was based on rotor No.3 by the Brookfield viscometer (the Tokyo Keiki Co., Ltd. make, DVL-B mold). In addition, a commercial solder resist constituent can also be used as a solder resist constituent.
[0139] (17) next, the upper layer — a conductor — the above-mentioned solder resist constituent was applied, for 20 minutes was performed at 70 degrees C, desiccation processing was performed to both sides of the

substrate in which the circuit 160 grade was formed, the condition for 30 minutes at 70 degrees C, and layer 62alpha of a solder REJISU constituent was formed in them (refer to drawing 6 (C)). Subsequently, the photo mask with a thickness of 5mm with which the pattern of opening was drawn was stuck to layer 62alpha of a solder resist constituent, it exposed by the ultraviolet rays of 1000 mJ/cm2, the development was carried out with the DMTG solution, and Openings 62a, 62b, and 62c were formed. and — further — it carries out at 120 degrees C for 1 hour for 1 hour, heat-treats [80 degrees C / 100 degrees C] on the conditions of 3 hours by 150 degrees C for 1 hour, respectively, and layer 62alpha of a solder resist constituent is hardened — making — a conductor — the solder resist layer 62 which has opening 62a which reaches a circuit 160, opening 62c which results in dummy pad 160c, and opening 62b for the substrate installation for optical element insertion was formed (refer to drawing 7 (A)).

[0140] (18) Next, the substrate 30 in which the solder resist layer 62 was formed was immersed in the non-electrolyzed nickel-plating liquid of pH=4.5 containing a nickel chloride (2.3x10-1 mol/l), sodium hypophosphite (2.8x10-1 mol/l), and a sodium citrate (1.6x10-1 mol/l) for 20 minutes, and the nickel-plating layer 66 with a thickness of 5 micrometers was formed in a part of opening 62a. The substrate 30 Furthermore, a gold cyanide potassium (7.6x10-3 mol/l), An ammonium chloride (1.9x10-1 mol/l), a sodium citrate (1.2x10-1 mol/l), It is immersed in the non-electrolyzed gilding liquid containing sodium hypophosphite (1.7x10-1 mol/l) for 7.5 minutes on 80-degree C conditions. On the nickel-plating layer 66, the pad 96 was formed by depositing the gilding layer 68 with a thickness of 0.03 micrometers, and it considered as the package substrate 10 (refer to drawing 7 (B)).

[0141] C. The laminating press by the production (1) mass lamination method of the substrate for IC chip mounting performed, and the substrate which stuck the substrate 100 (refer to drawing 2 (D)) for optical element insertion produced by Above A and the package substrate 10 (refer to drawing 7 (B)) produced by Above B through the adhesives layer 96 formed in the above-mentioned substrate 100 for optical element insertion obtained (refer to drawing 8 (A)). That is, after performing both alignment, a temperature up is carried out to 150 degrees C, and the substrate 100 for optical element insertion and the package substrate 10 were stuck by pressing in a pan by the pressure of 5MPa(s).

[0142] (20) On the other hand, prepare the solder resist layer which has opening 15a in the rear face of a light emitting device 12 and a photo detector 14 (drawing 13 (A) shows the side face and base of a light emitting device 12 in which the solder resist layer 15 equipped with opening 15a was formed).

(3) Attach 70gamma of soldering paste in opening 15a of the solder resist layer 15 of a light emitting device 12 and a photo detector 14 (drawing 13 (B) shows the side face and base of a light emitting device 12). In **, although soldering paste, such as Sn/Pb and Sn/Ag, is used, the die bond resin for various adhesion is applied. The metal paste with which the particle with the conductivity of resin, such as thermosetting resin, thermoplastics, and ultraviolet-rays hardening resin, copper, gold, silver, etc. was blended as die bond resin can use all things with adhesive strength. Soldering paste can also be applied to opening 62c of the solder resist layer prepared in the substrate side, although it applies to an optical element with 70gamma of soldering paste and the optical element concerned is mounted in a substrate in this example. Although there is especially no rule, as for the thickness (height) of soldering paste, it is desirable that it is the thickness of 5-100 micrometers. In less than 5 micrometers, if there is an adhesive fall and 100 micrometers is exceeded, a component will incline at the time of heat curing.

[0143] (4) Lay the photo detector 14 and light emitting device 12 which attached 70gamma of soldering paste in opening 62c of the package substrate 10 (refer to drawing 8 (B)). Here, as shown in drawing 13 (C) which is an enlarged drawing in the ellipse in drawing 8 (B), light sensing portion 14a and light-emitting part 12a are prepared in the top face of a photo detector 14 and a light emitting device 12, respectively. In addition, as a photo detector 14, what consists of InGaAsP was used as a light emitting device 12 using what consists of InGaAs.

[0144] (5) Once fusing 70gamma of soldering paste of 96.5Sn3.5Ag by performing a reflow at 250 degree C, fix a photo detector 14 and a light emitting device 12 to dummy pad 160c with solder 70 by cooling (refer to drawing 13 which expands and shows the inside of the ellipse in drawing 8 (C) and drawing 8 (C) (D)). In this case, the solder fused in the solder resist layer 15 of a photo detector 14 and a light emitting device 12 and the solder resist layer of the substrate 100 for IC chip mounting is flipped, solder is correctly settled in the location corresponding to opening 62c of the solder resist layer 62, and it is fixed to dummy pad 160c. With this, opening 62c of the solder resist layer 62 and opening 15a of a photo detector 14 and a light emitting device 12 counter, namely, the pin center,large of opening 62c and the pin center,large of a light emitting device [a photo detector 14 and] 12 of opening 15a correspond in order to move so that opening 15a of the solder resist layer 15 may come to the center section of solder (self-alignment). Thereby, the location of opening 62c of the solder resist layer 62 formed corresponding to the positioning mark (not shown) of a substrate, and a photo detector 14 and a light emitting device 12 suits. That is, a photo detector 14 and a light emitting device 12 can be arranged in a right location to the positioning mark (not shown) of a substrate. In addition, opening 15a which prepares

70gamma of soldering paste is the three or more place need. This is for making it a light emitting device 12 and a photo detector 14 not incline in the case of the above-mentioned solder reflow. It is most desirable to prepare three openings from a viewpoint of economical efficiency especially.

[0145] (6) Next, 12d of electrodes of a photo detector 14 and a light emitting device 12 and the pad 96 of the front face of a package substrate were connected by wirebonding (refer to drawing 9 (A)). Here, the wire made from Au was used as a wire 72. As a wire 72 used, metal wires, such as silver and aluminum, can be used besides Au, and a 15-50-micrometer thing can be used for line breadth. a component side — ball bonding — carrying out — a conductor — a circuit side is connected by performing wedge bonding.

[0146] (7) Next, the solder resist constituent prepared at the process of (16) of production of the above-mentioned package substrate and the same resin constituent were prepared, this was applied to the substrate side for optical element insertion of a substrate, for 20 minutes was performed at 70 degrees C, desiccation processing was performed the condition for 30 minutes at 70 degrees C, and layer 76alpha of a solder resist constituent was formed (refer to drawing 9 (B)). In addition, a solder resist constituent was not applied in the through tube 98 here.

[0147] Subsequently, the photo detector 14 was positioned as an alignment mark, the photo mask (not shown) with a thickness of 5mm with which the pattern of opening was drawn was stuck to layer 76alpha of a solder resist constituent, it exposed by the ultraviolet rays of 1000 mJ/cm2, the development was carried out with the DMTG solution, and opening 76a was formed (refer to drawing 9 (C)). In addition, opening 76b of the center of a solder resist layer was formed so that it might become larger than a through tube 98. The top view of the substrate for IC chip mounting shown in drawing 9 (C) is shown in drawing 14 . In this example, since a photo detector 14 is used as an alignment mark, the relative position of a photo detector 14 and opening 76a can be doubled correctly.

[0148] And further, it carried out at 120 degrees C for 1 hour for 1 hour, heat-treated [80 degrees C / 1 hour and 100 degrees C] on the conditions of 3 hours by 150 degrees C, respectively, layer 76alpha of a solder resist constituent was stiffened, and the solder resist layer 76 which has opening 76a was formed. Therefore, when this process is finished, the solder resist layer 76 will be formed in the substrate side for optical element insertion, and the solder resist layer 62 will be formed in the package substrate side, respectively. Here, although opening 76a was prepared by exposure and development, a photo detector 14 can be positioned as an alignment mark, and opening 76a can also be prepared by laser.

[0149] (8) Next, it was filled up with the resin constituent containing an epoxy resin by printing in the through tube 98 formed in the substrate for optical element insertion, and this resin constituent was dried after that. Furthermore, buffing and mirror polishing were given to the exposure of a resin constituent. Then, it heat-treated and considered as the resin packed bed 74 (refer to drawing 9 (B)). In addition, the permeability of the perpendicular direction of wavelength the light of 1.55 micrometers of the resin packed bed 74 is 93%.

[0150] In this example, the edge of a photo detector 14 or a light emitting device 12 or the mirror (light sensing portion 14a, light-emitting part 12a) of a component was used as an alignment mark on the occasion of positioning. Instead an alignment mark can be formed at a photo detector 14 or a light emitting device 12, and this alignment mark can also be used for positioning. By it, spacing of the solder bump (or solder pad) and photo detector 14 which are formed in opening 76a becomes a desired thing, the pad location of the external substrate of a solder bump (solder pad) and a receptacle becomes exact, and the location of a photo detector and optical waveguide also becomes exact. It is effective in the ability of transfer of a lightwave signal and an electrical signal to carry out correctly.

[0151] Although the photo detector of a wire-bonding mold explains the above, it can use as an alignment mark also by the photo detector of a FIRIPPU chip mold. In that case, after filling up closure resin with a solder bump into what connected the photo detector, a solder pad is made to form as an alignment mark like the above.

[0152] (9) Next, the substrate was immersed in the non-electrolyzed nickel-plating liquid of pH=4.5 containing a nickel chloride (2.3x10-1 mol/l), sodium hypophosphite (2.8x10-1 mol/l), and a sodium citrate (1.6x10-1 mol/l) for 20 minutes, and the nickel-plating layer 77 with a thickness of 5 micrometers was formed in a part of opening 76a. Furthermore, the substrate was immersed in the non-electrolyzed gilding liquid containing a gold cyanide potassium (7.6x10-3 mol/l), an ammonium chloride (1.9x10 to 1 mol/l.), a sodium citrate (1.2x10-1 mol/l), and sodium hypophosphite (1.7x10-1 mol/l) for 7.5 minutes on 80-degree C conditions, and the gilding layer 78 with a thickness of 0.03 micrometers was formed on the nickel-plating layer 77 (refer to drawing 10 (B)).

[0153] (11) It is on the perpendicular of light sensing portion 14a of a photo detector 14, and light-emitting part 12a of a light emitting device 12, and attach a micro lens 99 in the front face of the resin packed bed 74 (refer to drawing 1010 (C)). A micro lens 99 can also stick on the resin packed bed 74 with adhesives the micro lens which applying by the dispenser, the ink jet, micro PIPETSU, etc. also formed beforehand with injection molding.

[0154] (12) Next, soldering paste was printed to opening 76a formed in the solder resist layer 76, and opening

62a which the solder resist layer 62 has, by carrying out a reflow at 200 degrees C, the solder bumps (or BGA, a conductive contact pin) 79U and 79D were formed, and the substrate 20 for IC chip mounting was obtained (refer to drawing 11).

[0155] Thus, IC chip is carried in the obtained substrate 20 for IC chip mounting. First, by carrying out alignment of the IC chip 102 by the positioning mark which the substrate 20 for IC chip mounting does not illustrate, and the positioning mark by the side of the IC chip 102 (not shown), it lays so that the pad 104 of the IC chip 102 concerned may correspond to solder bump (or BGA) 79D of the substrate 20 for IC chip mounting. And it carries in the substrate 20 for IC chip mounting by performing a reflow. Next, by carrying out alignment by the positioning mark and the positioning mark (not shown) of the DOTA board 108 which the substrate 20 for IC chip mounting concerned does not illustrate, the substrate 20 for IC chip mounting carrying the IC chip 102 is laid so that solder bump 79U of the substrate 20 for IC chip mounting concerned may correspond to the pad 106 of a DOTA board. and reflow **** — the substrate 20 for IC chip mounting is carried in the DOTA board 108 by things.

[0156] although the example which carries the photo detector of a pair and a light emitting device in the crevice of the substrate for IC chip mounting was given in this example — these either — or it can also have more than one. Furthermore, the plurality of a photo detector, a driver component and a light emitting device, and a driver component / amplifier component may be mounted.

[0157] [2nd example] drawing 16 shows the substrate for IC chip mounting concerning the 2nd example of this invention. In this 2nd example, a photo detector 14 and a light emitting device 12 are mounted in a substrate front face, and resin 74 is closed through the dam substrate 114 stuck through adhesives 112. the conductor which mainly connects a photo detector and IC chip to a photo detector 14 side also in this 2nd example — the conductor which arranges a circuit and mainly connects a light emitting device and IC chip to a light emitting device 12 side — the circuit is arranged.

[0158] [3rd example] drawing 17 shows the substrate for IC chip mounting concerning the 3rd example of this invention. Although electrical connection of a photo detector 14, a light emitting device 12, and the substrate was carried out in the 1st example using the bonding wire 72, FIRIPPU chip mounting of a photo detector 14 and the light emitting device 12 is carried out to the substrate in this 3rd example. the conductor which mainly connects a photo detector and IC chip to a photo detector 14 side also in this 2nd example — the conductor which arranges a circuit and mainly connects a light emitting device and IC chip to a light emitting device 12 side — the circuit is arranged.

[0159]

[Effect of the Invention] the conductor which mainly connects a light emitting device and IC chip to a multilayer printed wiring board light emitting device loading-side in the substrate for optical element mounting of this invention as explained above — the conductor which arranges a circuit and mainly connects a photo detector and IC chip to a multilayer printed wiring board photo detector loading-side — a circuit is arranged. for this reason, the conductor which connects a photo detector and IC chip — the conductor which connects the die length, and a light emitting device and IC chip of a circuit — the die length of a circuit becomes short and a photo detector, a light emitting device, and IC chip can be connected rationally. moreover, the conductor which transmits the input from a photo detector — the conductor which delivers the output to a light emitting device a circuit — effect of a noise etc. can be made hard to separate I/O and to affect it, in order to divide and arrange a circuit within a multilayer printed wiring board.

[Translation done.]

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DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] (A) – (E) is the fragmentary sectional view showing typically the process which produces the substrate for optical element insertion in the manufacture approach of the substrate for IC chip mounting concerning the 1st example.
[Drawing 2] (A) – (D) is the fragmentary sectional view showing typically the process which produces the substrate for optical element insertion in the manufacture approach of the substrate for IC chip mounting concerning the 1st example.
[Drawing 3] (A) – (E) is the fragmentary sectional view showing typically a part of process which produces the package substrate in the manufacture approach of the substrate for IC chip mounting concerning the 1st example.
[Drawing 4] (A) – (E) is the fragmentary sectional view showing typically a part of process which produces the package substrate in the manufacture approach of the substrate for IC chip mounting concerning the 1st example.
[Drawing 5] (A) – (D) is the fragmentary sectional view showing typically a part of process which produces the package substrate in the manufacture approach of the substrate for IC chip mounting concerning the 1st example.
[Drawing 6] (A) – (C) is the fragmentary sectional view showing typically a part of process which produces the package substrate in the manufacture approach of the substrate for IC chip mounting concerning the 1st example.
[Drawing 7] (A) and (B) are the fragmentary sectional views showing typically a part of process which produces the package substrate in the manufacture approach of the substrate for IC chip mounting concerning the 1st example.
[Drawing 8] (A) – (C) is the fragmentary sectional view showing typically a part of manufacture approach of the substrate for IC chip mounting concerning the 1st example.
[Drawing 9] (A) – (C) is the fragmentary sectional view showing typically a part of manufacture approach of the substrate for IC chip mounting concerning the 1st example.
[Drawing 10] (A) – (C) is the fragmentary sectional view showing typically a part of manufacture approach of the substrate for IC chip mounting concerning the 1st example.
[Drawing 11] It is the fragmentary sectional view showing typically some substrates for IC chip mounting concerning the 1st example.
[Drawing 12] It is the fragmentary sectional view showing typically the condition of having carried IC chip in the substrate for IC chip mounting concerning the 1st example, and having attached in the DOTA board.
[Drawing 13] (B) is the side elevation and bottom view of a light emitting device after soldering paste installation, (A) is the side elevation and bottom view of a light emitting device before soldering paste installation, and (D) is [(C) is the expansion fragmentary sectional view expanding and showing the ellipse part of drawing 8 (B), and] the expansion fragmentary sectional view expanding and showing the ellipse part of drawing 8 (C).
[Drawing 14] It is the top view of the substrate for IC chip mounting shown in drawing 10 (A).
[Drawing 15] It is the top view of the substrate for IC chip mounting shown in drawing 11 .
[Drawing 16] It is the fragmentary sectional view showing typically some substrates for IC chip mounting concerning the 2nd example.
[Drawing 17] It is the fragmentary sectional view showing typically some substrates for IC chip mounting concerning the 3rd example.
[Description of Notations]
10 Package Substrate
12 Light Emitting Device

12a Light-emitting part
14 Photo Detector
14a Light sensing portion
15 Solder Resist Layer
15a Opening
20 Substrate for IC Chip Mounting
16 Optical Waveguide
18 Optical Waveguide
22 Resin Insulating Layer between Layers
23 Plating Resist
30 Substrate
32 Copper Foil
36 Through Hole
40 Resin Packed Bed
50 Resin Insulating Layer between Layers
58 Bahia Hall
60 Conductor — Circuit
62 Solder Resist Layer
62a Opening
70 Solder
70gamma Soldering paste
79U, 79D Solder bump
94 Lid Plating Layer
98 Through Tube
100 Substrate for Optical Element Insertion
102 IC Chip
108 DOTA Board
160c Dummy pad

[Translation done.]

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